Quantum-size effects in sub-10 nm fin width InGaAs finFETs

Alon Vardi, Xin Zhao, and Jesús A. del Alamo

Microsystems Technology Laboratories, MIT

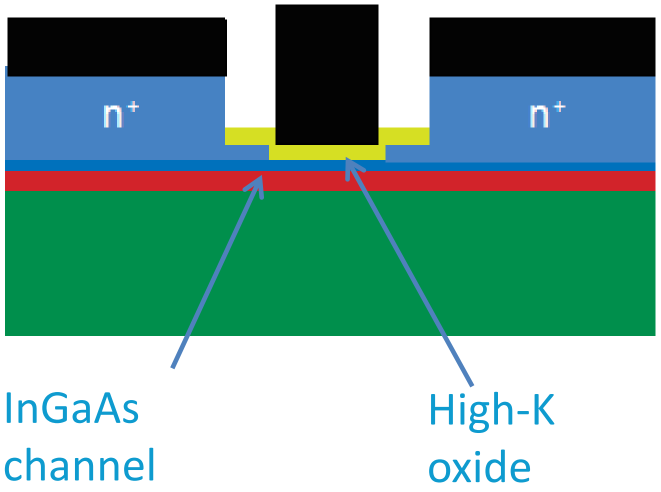
December 9, 2015

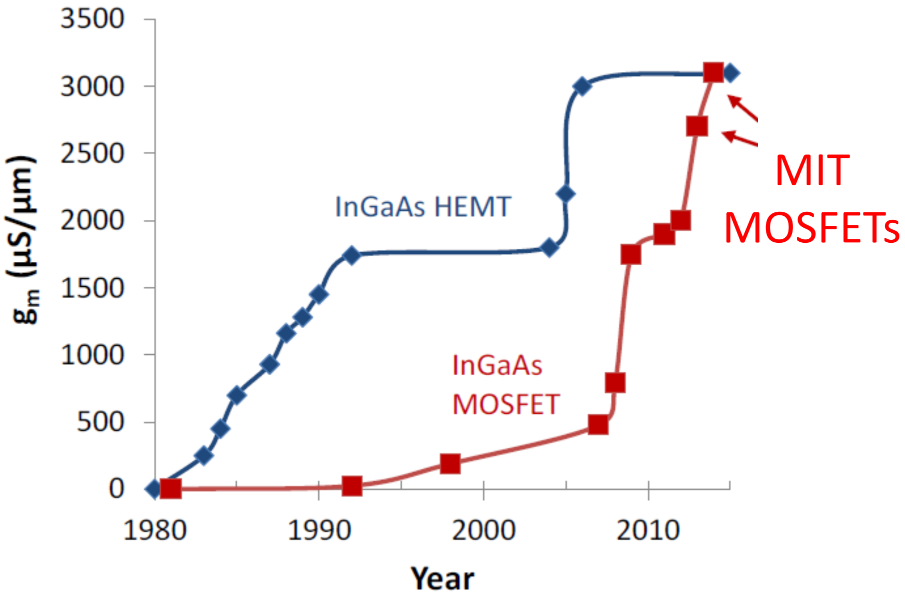
Sponsors:
DTRA
NSF (E3S STC)
Northrop Grumman

Outline

- Motivation
- Process Technology
- Electrical characteristics
- Modeling
- Conclusions

InGaAs planar Quantum-Well MOSFETs

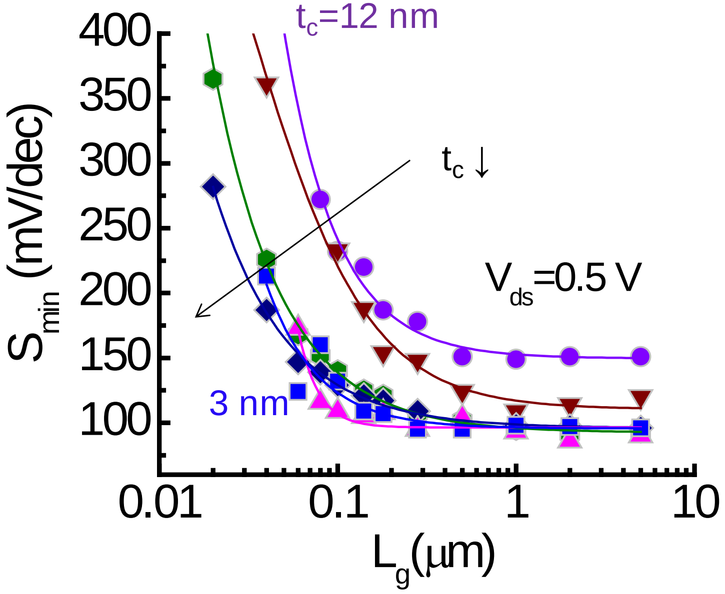


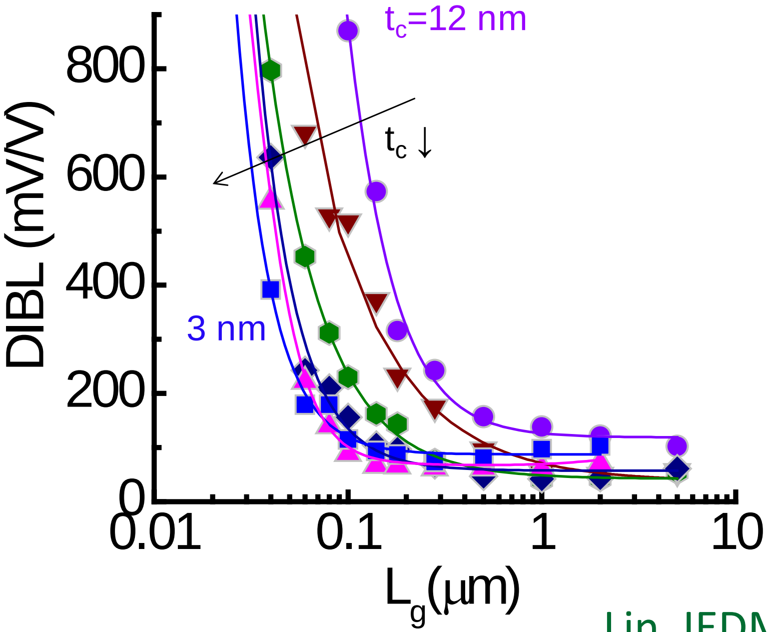


del Alamo, CSICS 2015

- InGaAs planar MOSFET performance matches that of High Electron Mobility Transistors (HEMT)

InGaAs planar Quantum-Well MOSFETs - short-channel effects

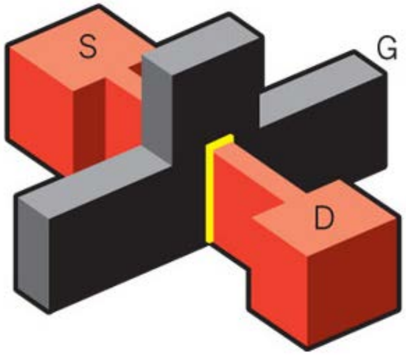


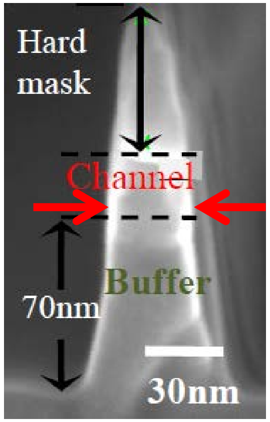


Lin, IEDM 2014

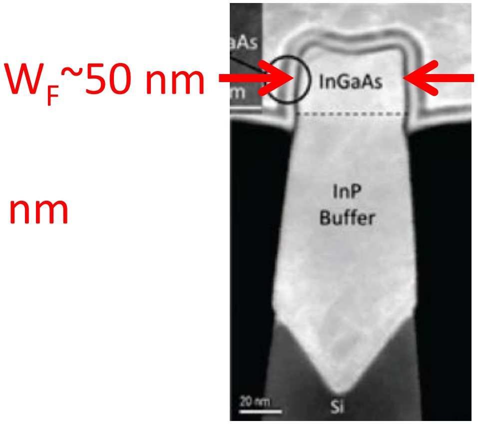
- Short-channel effects limit scaling to L_g~40 nm
- 3D transistors required for further scaling

InGaAs finFETs

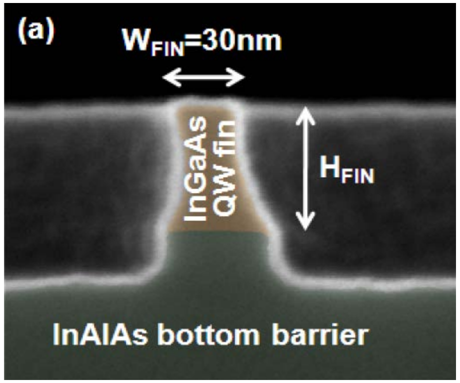




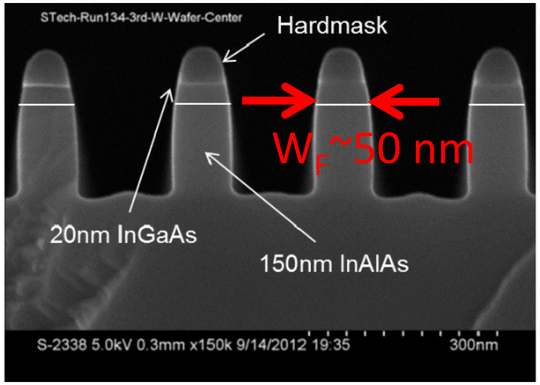
Thathachary, VLSI 2015



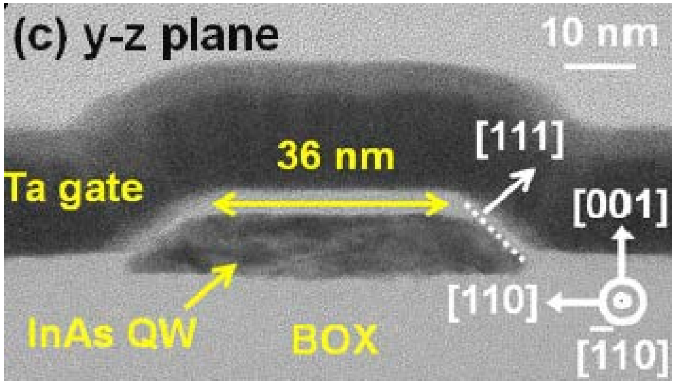
Waldron, VLSI 2014



Radosavljevic ,IEDM 2011



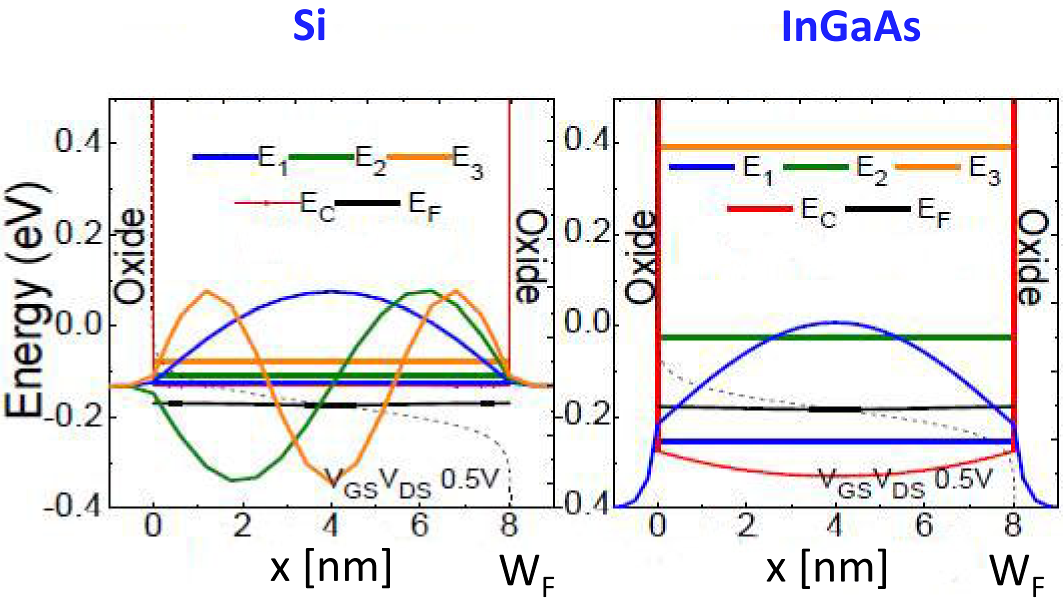
Kim, IEDM 2013



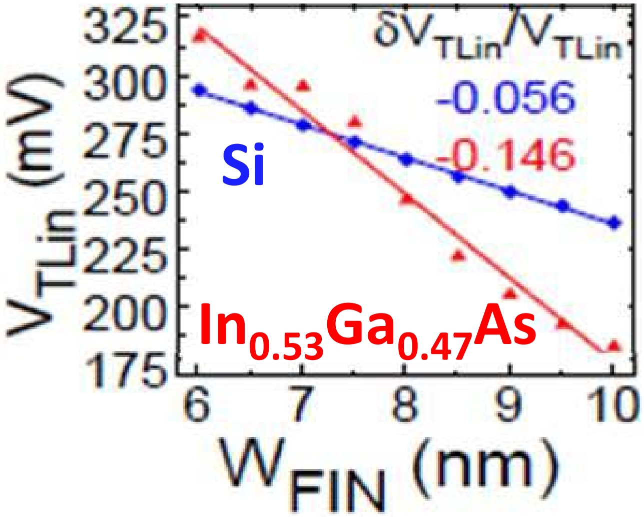
Kim, TED 2014

- III-V finFETs improve short-channel effects
- Most InGaAs finFETs demonstrations feature W_f=30-50 nm

V_T variation with W_f



Increased sensitivity of V_T to W_F in InGaAs



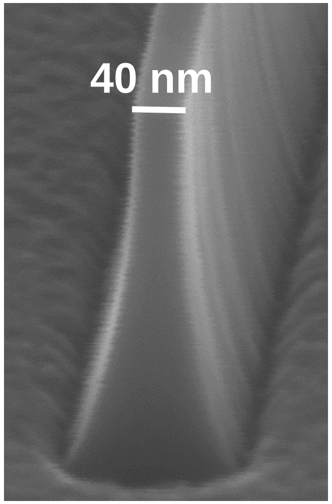
Nidhi, DRC 2012

- m^*_e(Si)/m^*_e(InGaAs) >7 → Quantum effects ↑ → ΔV_T(InGaAs) ↑
- Goal of this work: experimental verification
- Need InGaAs finFET with W_f<10 nm

Key technologies – nanostructure definition – Dry etch

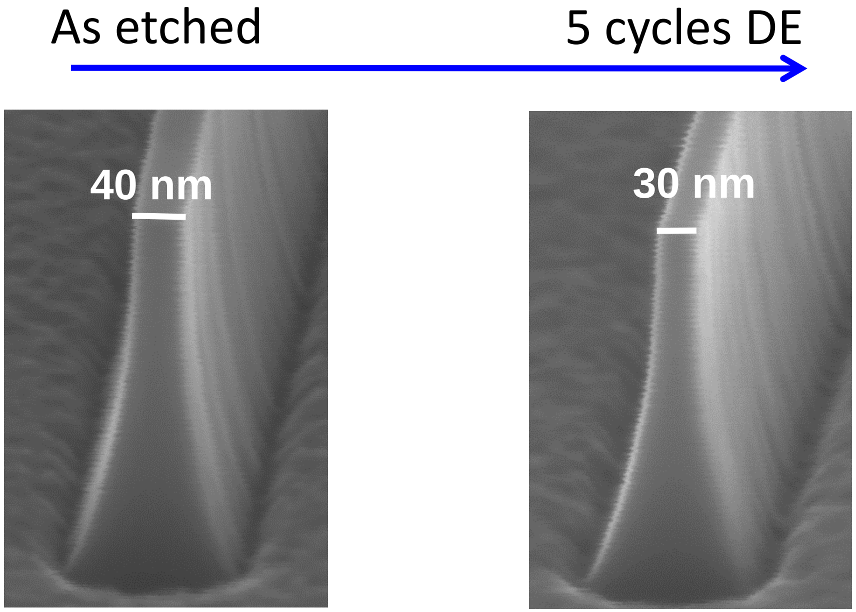
- **BCl_3/$SiCl_4$/Ar RIE** of InGaAs nanostructures with smooth, vertical sidewalls and high aspect ratio (>10)

As etched



Key technologies – nanostructure definition – Digital etch (DE)

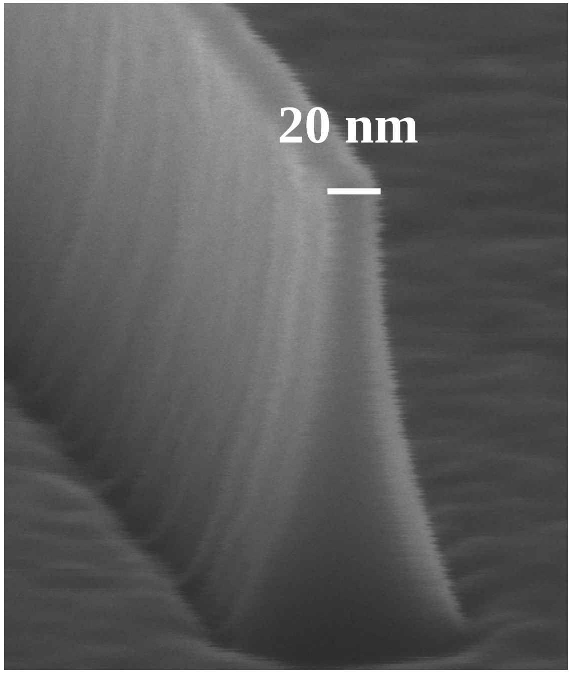
- **Digital etch (DE)**: self-limiting O_2 plasma oxidation + H_2SO_4 oxide removal

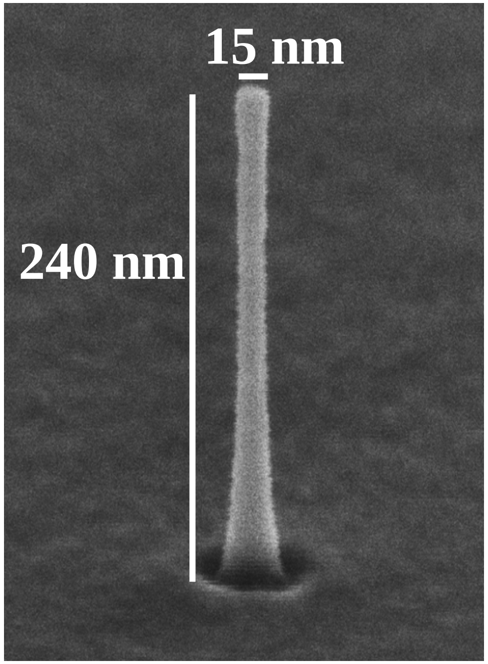


Lin, EDL 2014

- Shrinks fin width by 2 nm per cycle
- Unchanged shape
- Reduced roughness

Key technologies – nanostructure definition
Dry etch + Digital etch



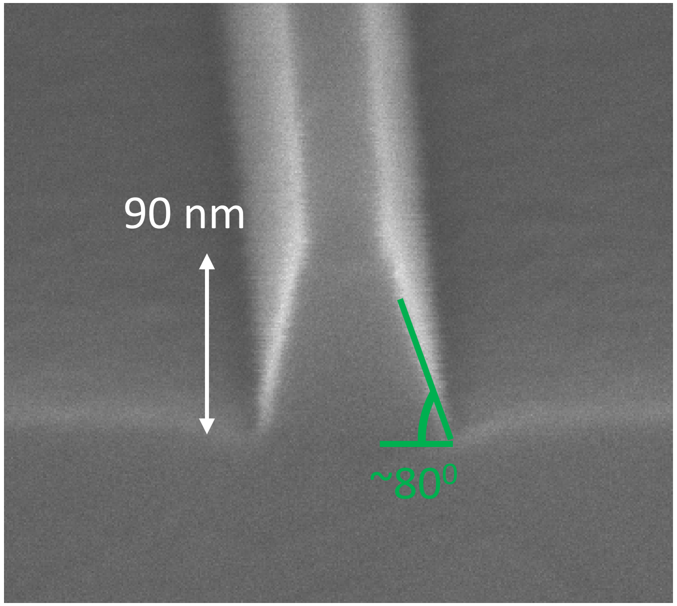


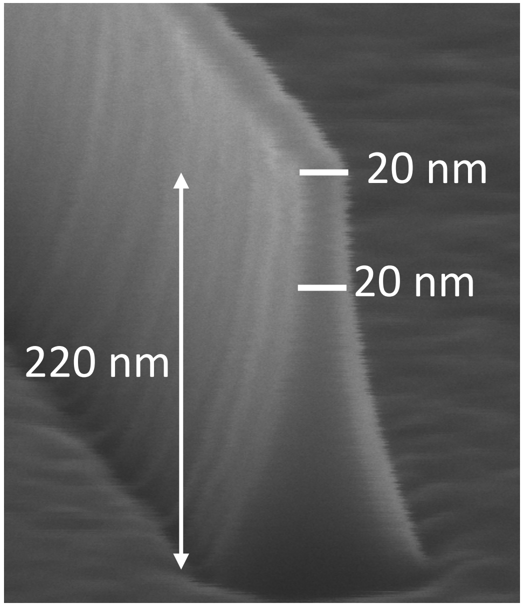
Zhao, EDL 2014

Stand alone nano structures down to 15 nm

Key technologies – nanostructure definition – sidewall slope

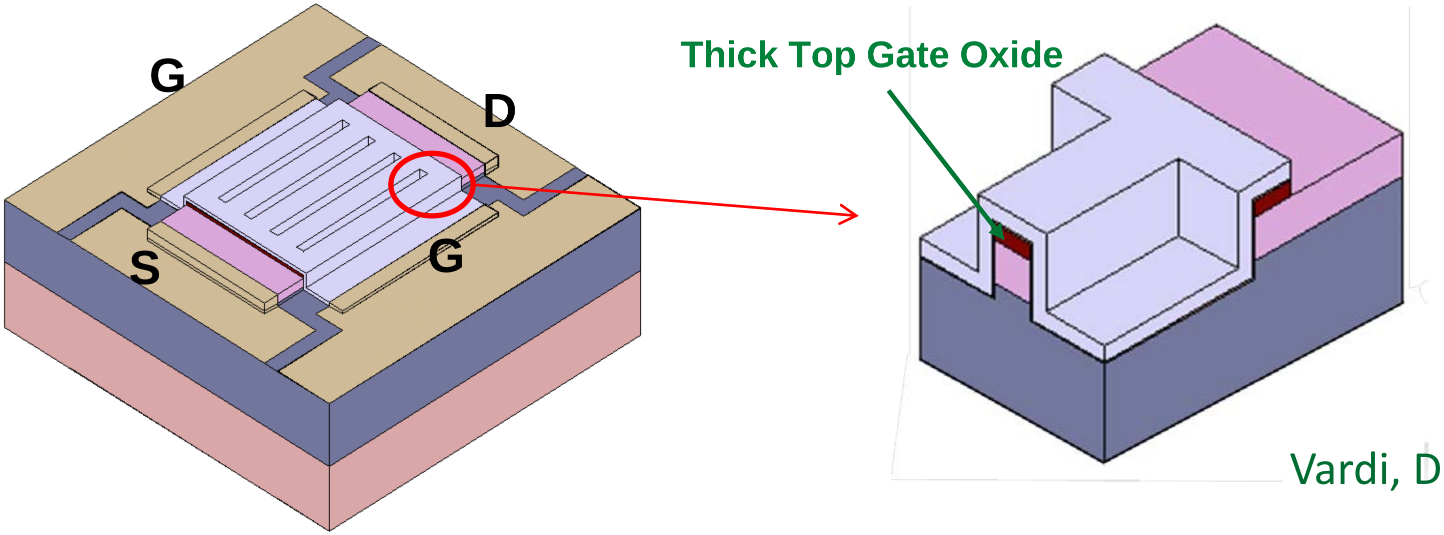
Etching time →



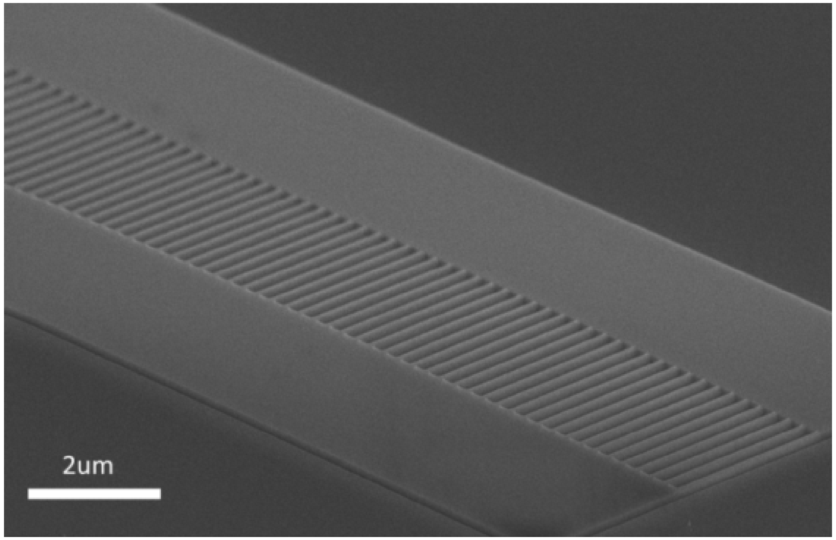


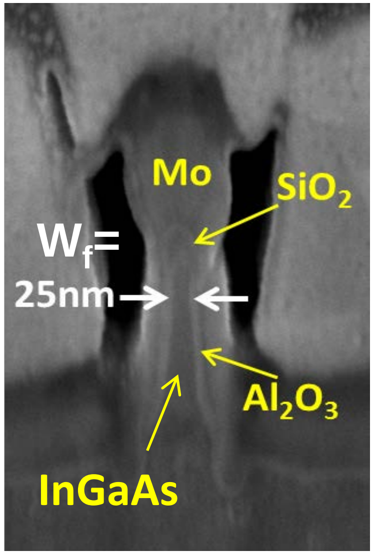
- Etching depth impacts sidewall slope at top 50 nm
- For H_f > 150 nm, upper 50 nm sidewalls become vertical

Sidewall finFET



Vardi, DRC 2014

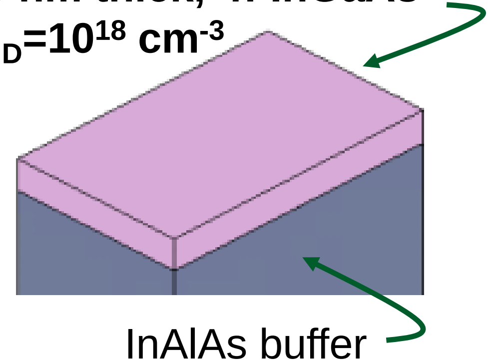




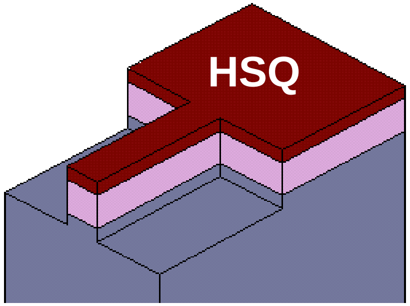
- Typical device consists of 100 fins, L_g=3 μm

Sidewall finFET - process flow

50 nm thick, n-InGaAs
$N_D=10^{18}$ cm^{-3}

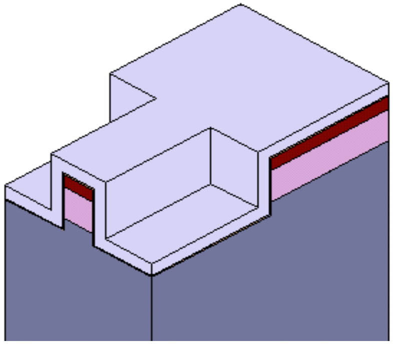


InAlAs buffer
on SI-InP

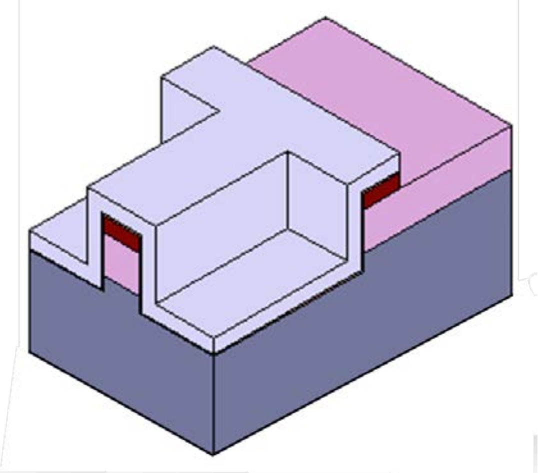


Fin Patterning + Digital etch

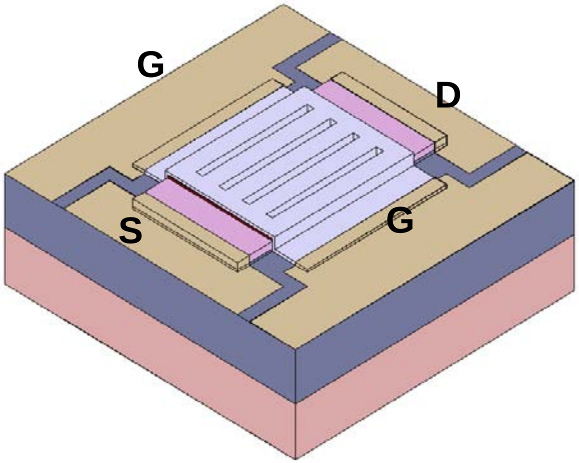
Gate dielectric + Mo



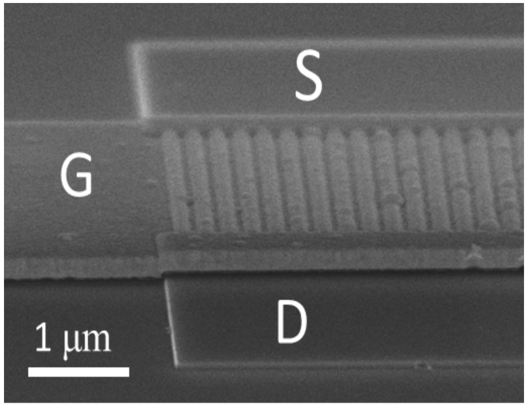
Gate stack



Gate Patterning →



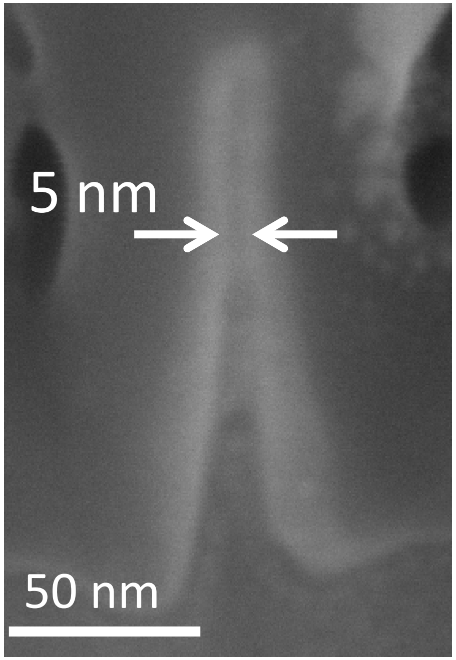
Contacts + Pads



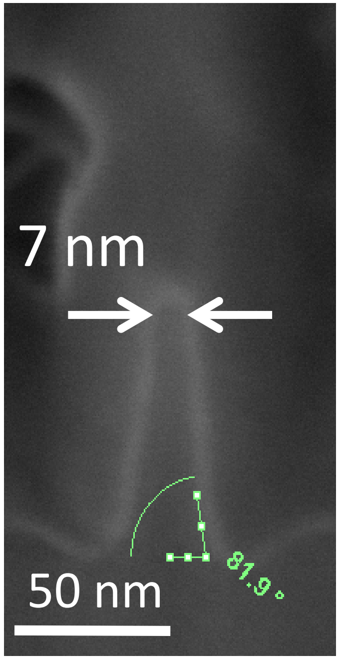
Sub-10 nm fin-width InGaAs finFETs

- 50 nm thick InGaAs channel
- $N_D=10^{18}$ cm^{-3}
- $L_g=3$ μm
- Oxide: Al_2O_3/HfO_2 (EOT~3 nm)

SW ~ 90°

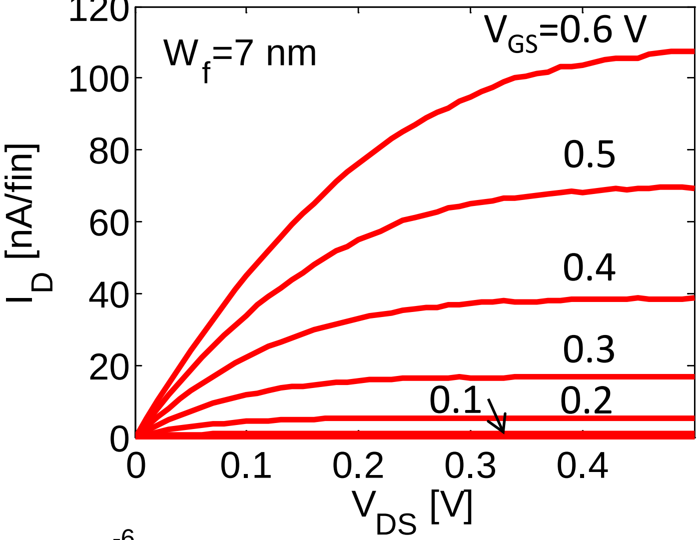


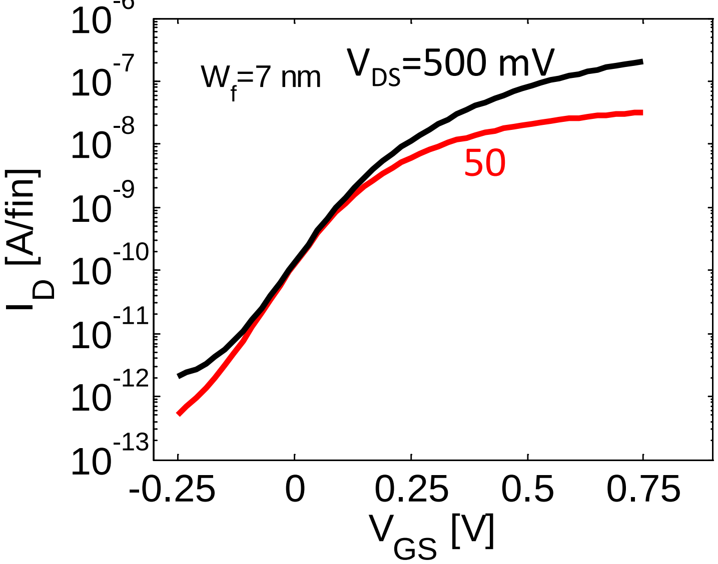
SW ~ 80°



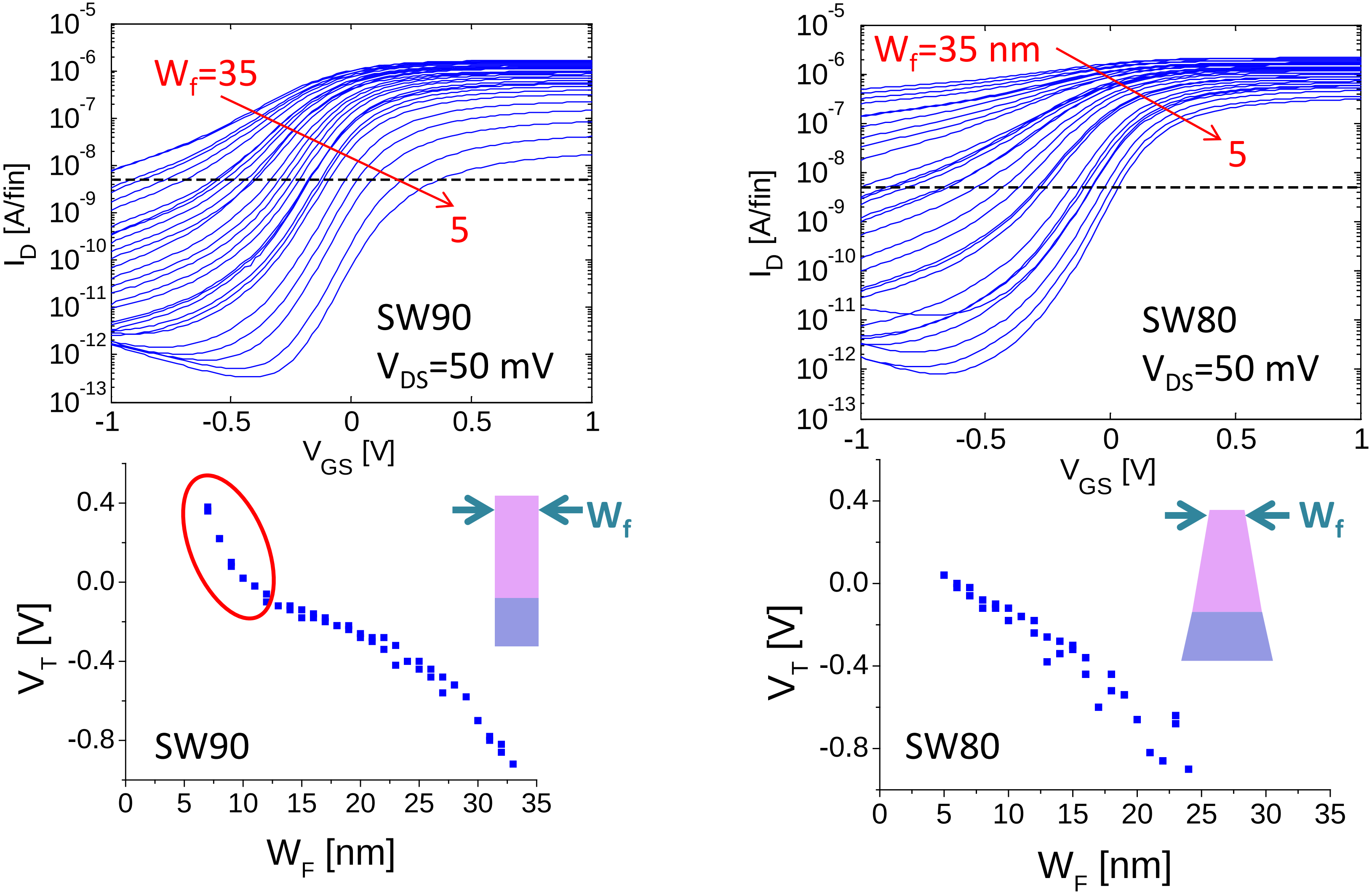
$W_f=7$ nm, $L_g=3$ μm MOSFET

(SW ~ 90°)



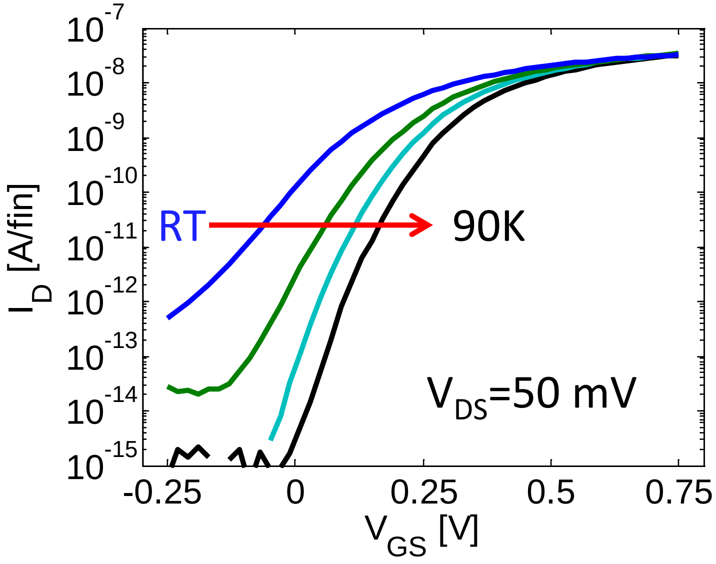


Impact of W_f on subthreshold characteristics



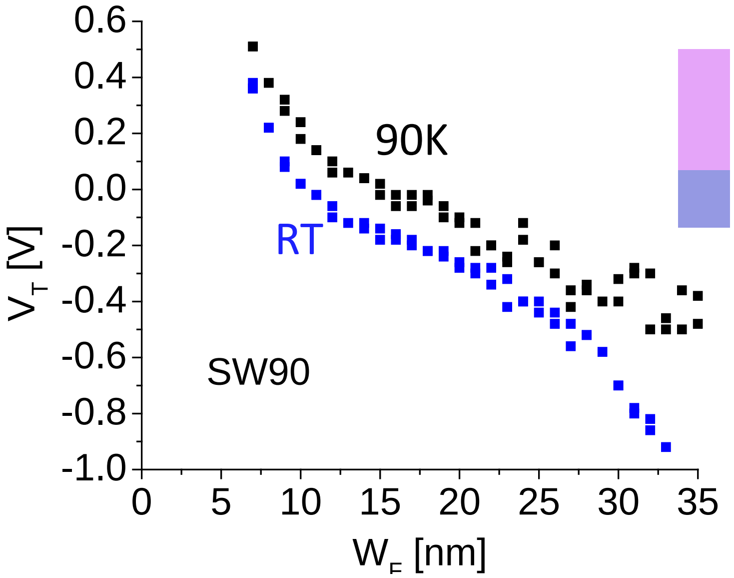
- V_T defined at 5 nA/fin
- Strong sensitivity of V_T to W_f<10 nm for SW90

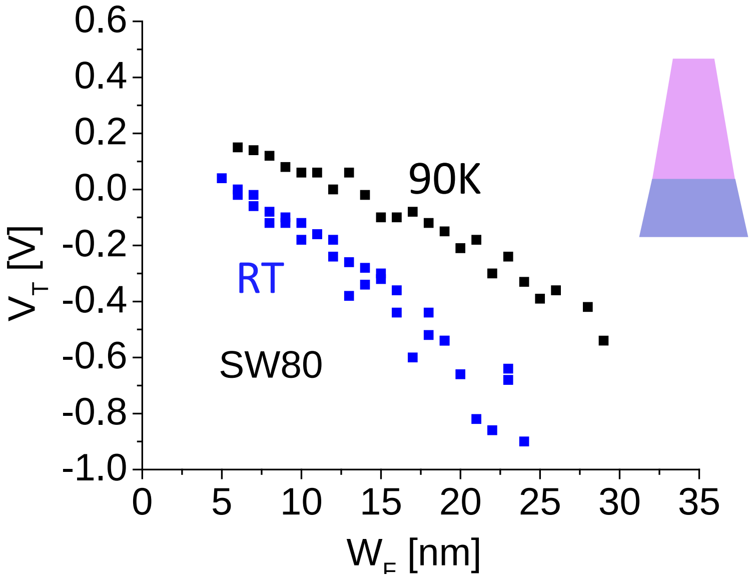
Low-temperature measurements



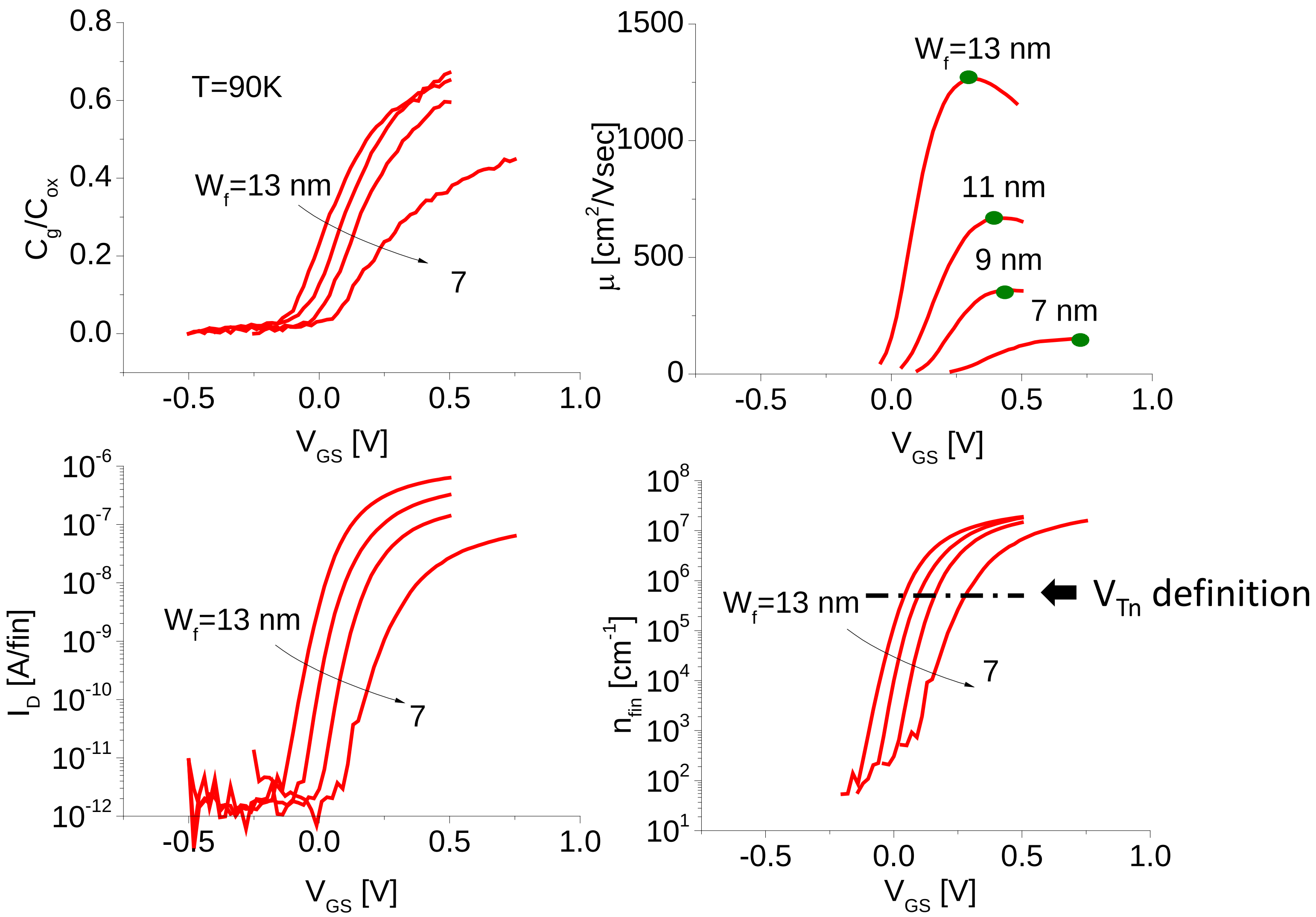
as T↓ →

- D_{it} impact ↓
- Rigid $\Delta V_T > 0$
- Strong sensitivity of V_T to W_f for SW90 maintained





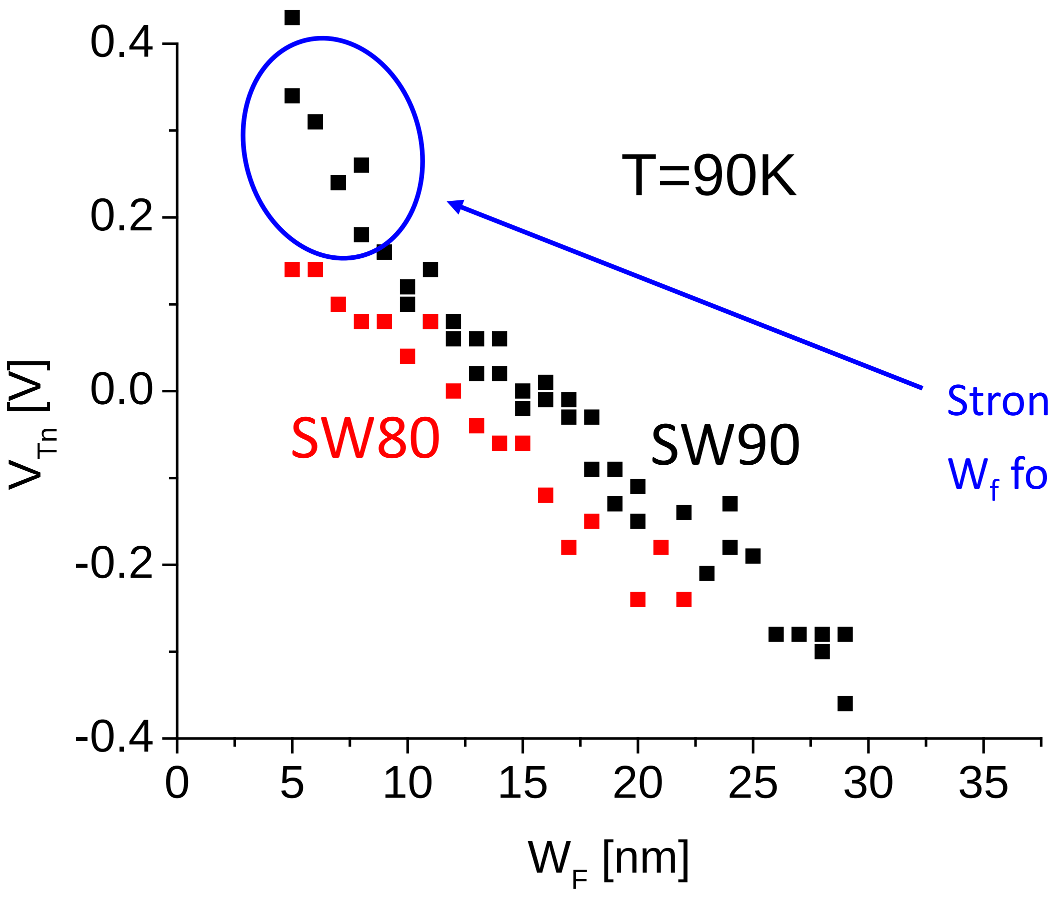
Subthreshold carrier concentration at 90K



- CV+IV → μ(V_{GS})
- Use μ_{max} to transfer subthreshold characteristics to n_{fin}

Impact of W_f on V_T

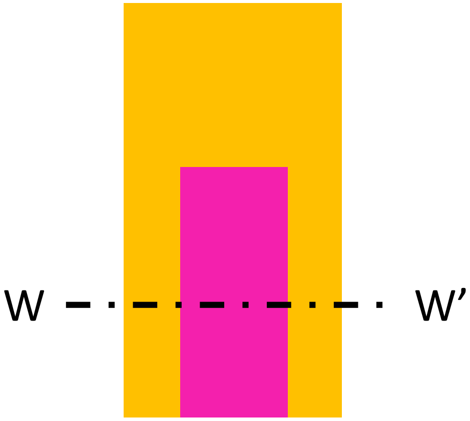
V_{Tn} at constant $n_{fin}=5\cdot 10^5$ cm^{-1}

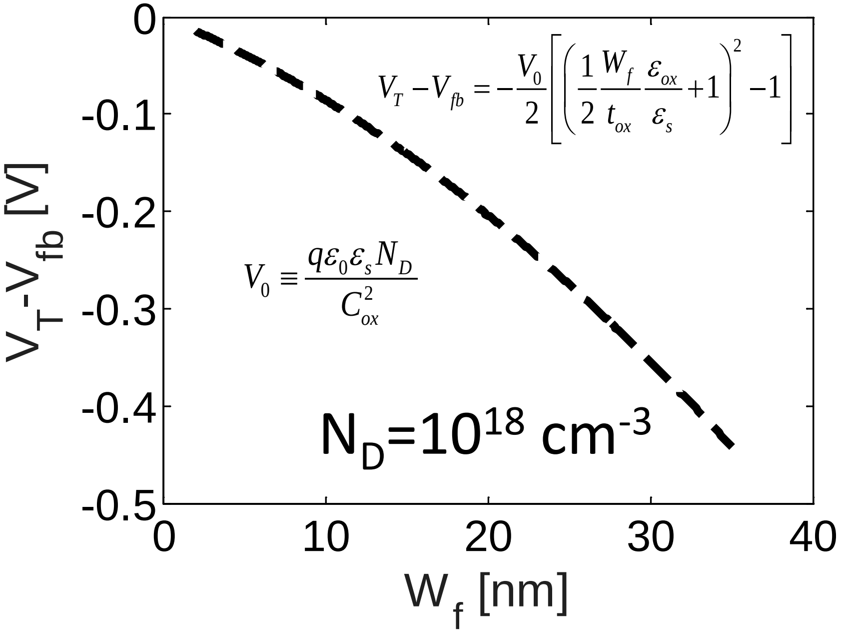


Strong sensitivity of V_T to W_f for SW~90° MOSFETs

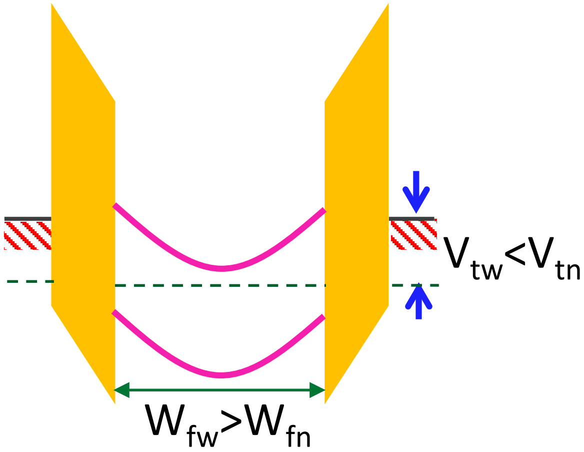
V_{Tn} sensitivity to W_f persists

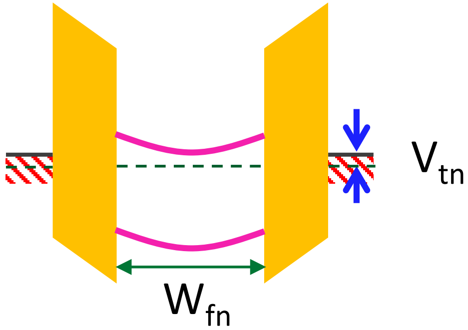
Classic V_T – W_f dependence





Threshold:

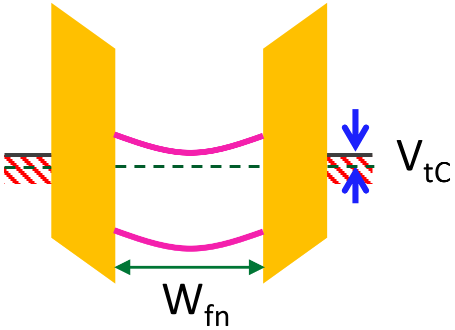




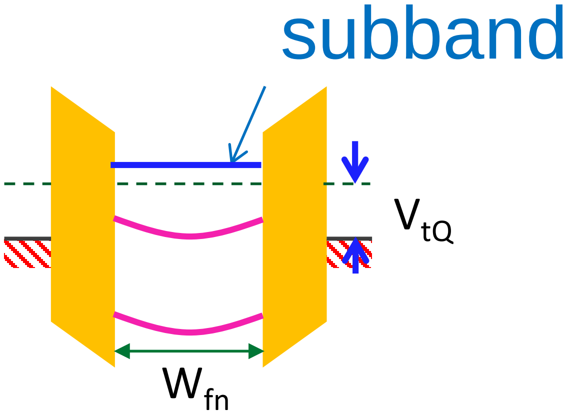
- $W_f \uparrow \rightarrow |V_T - V_{fb}| \uparrow$

Quantum V_T – W_f dependence

Classic



Quantum

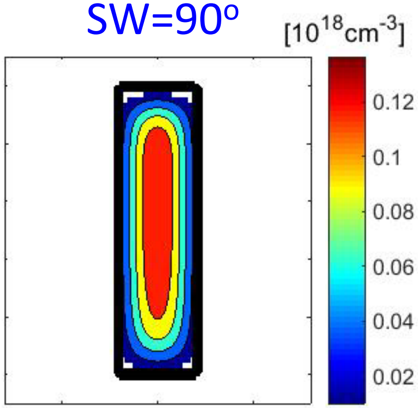


- Quantum confinement creates subbands → CB Min↑
- For constant N_D → E_F ↑
- Positive shift to V_T as W_f↓

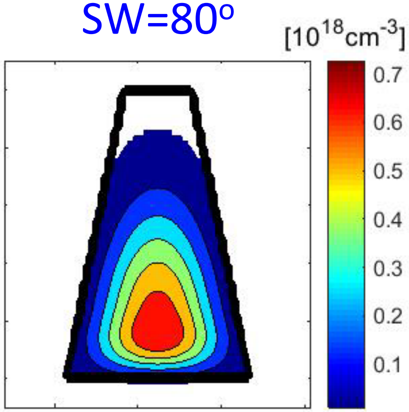
Impact of W_f on V_T

Poisson-Schrodinger simulations (Nextnano):

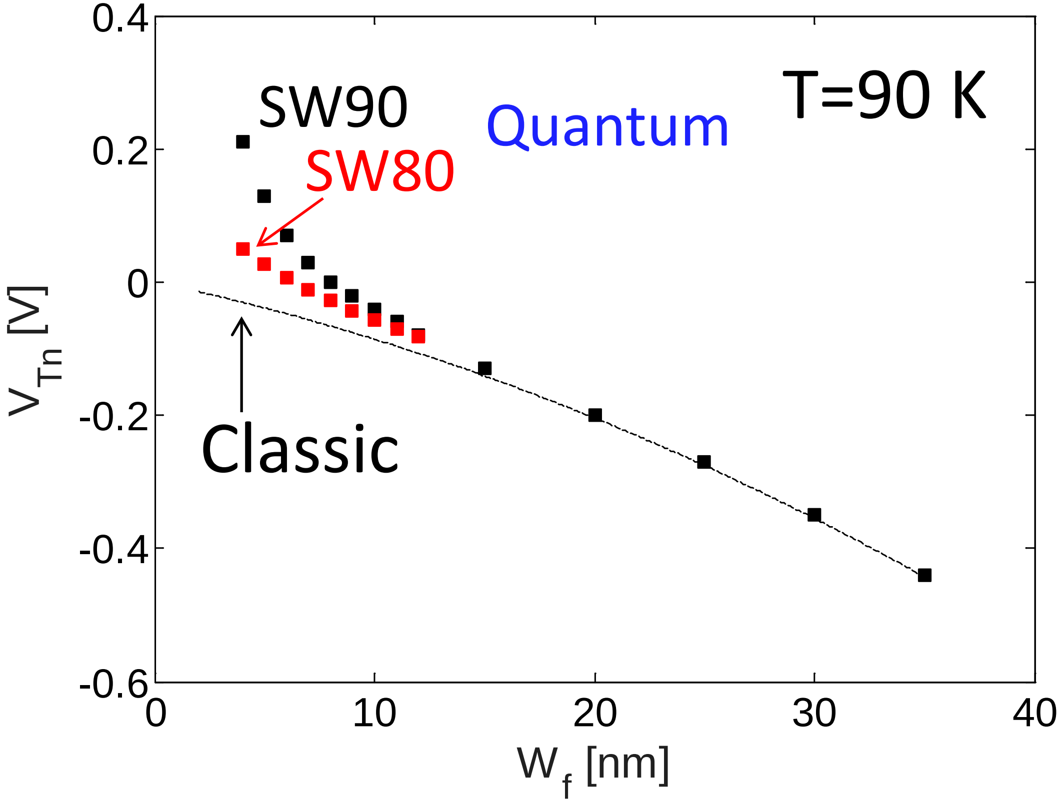
SW=90°



SW=80°



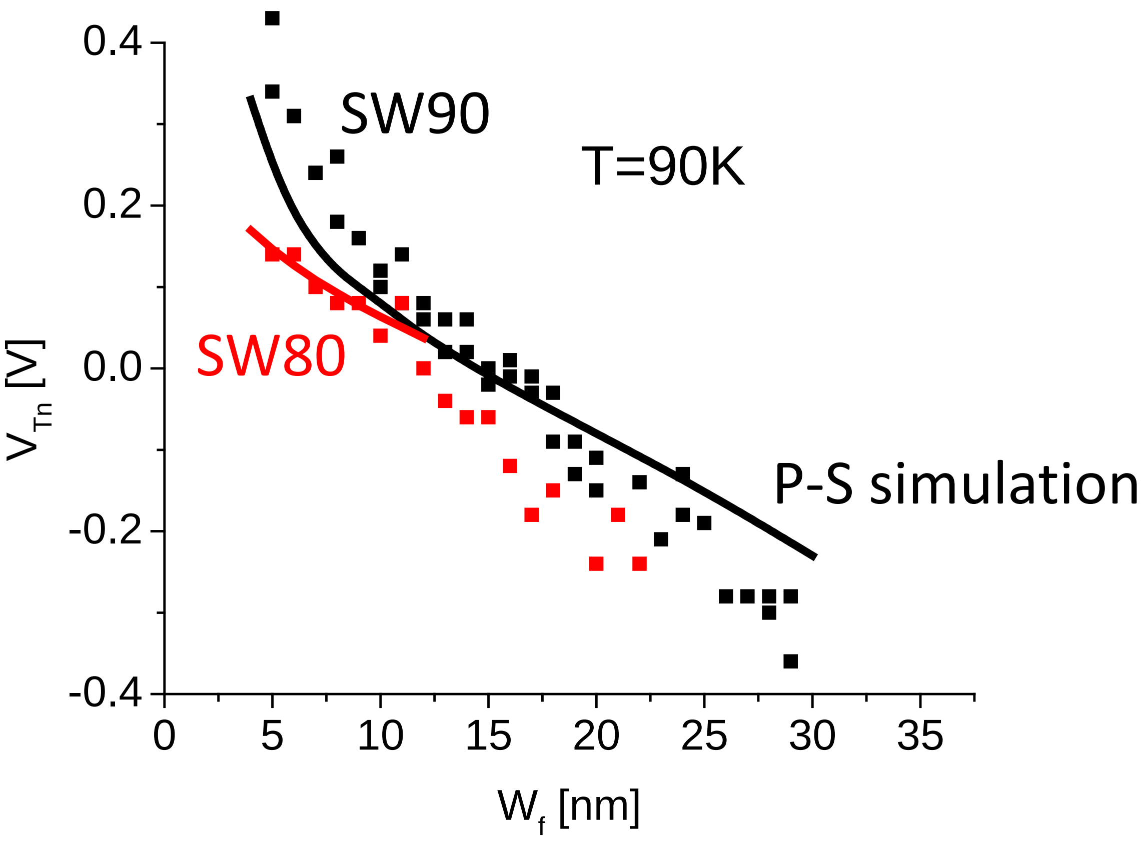
$W_f = 4$nm



- $\Delta V_T > 0$ due to quantum confinement for $W_f < 10$ nm
- Larger ΔV_T in SW90 due to greater quantum confinement

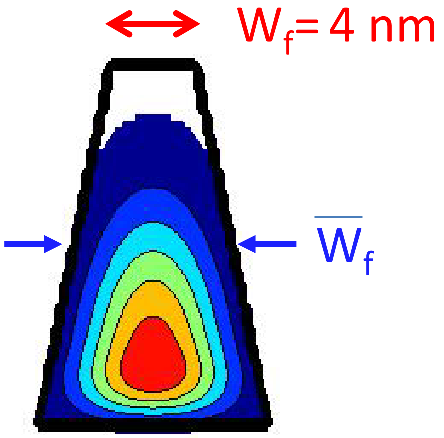
Impact of W_f on V_T

Comparison of simulation and experiments:

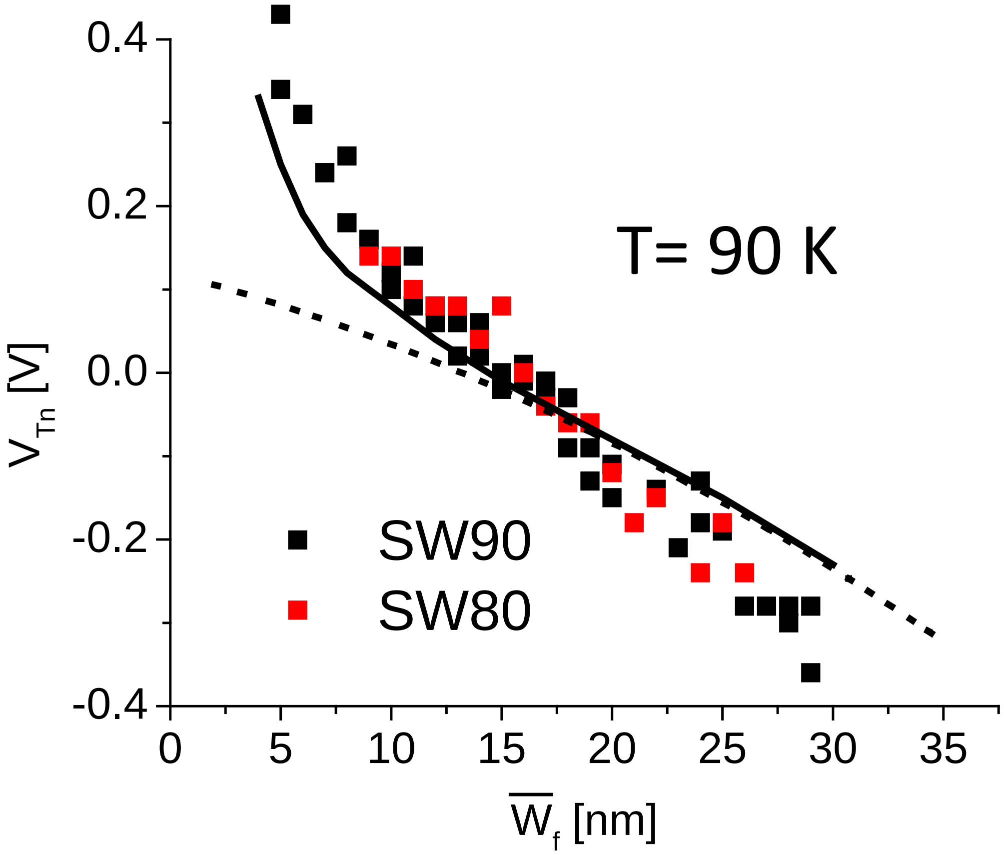


Good agreement after rigid V_T shift

Impact of sidewall slope

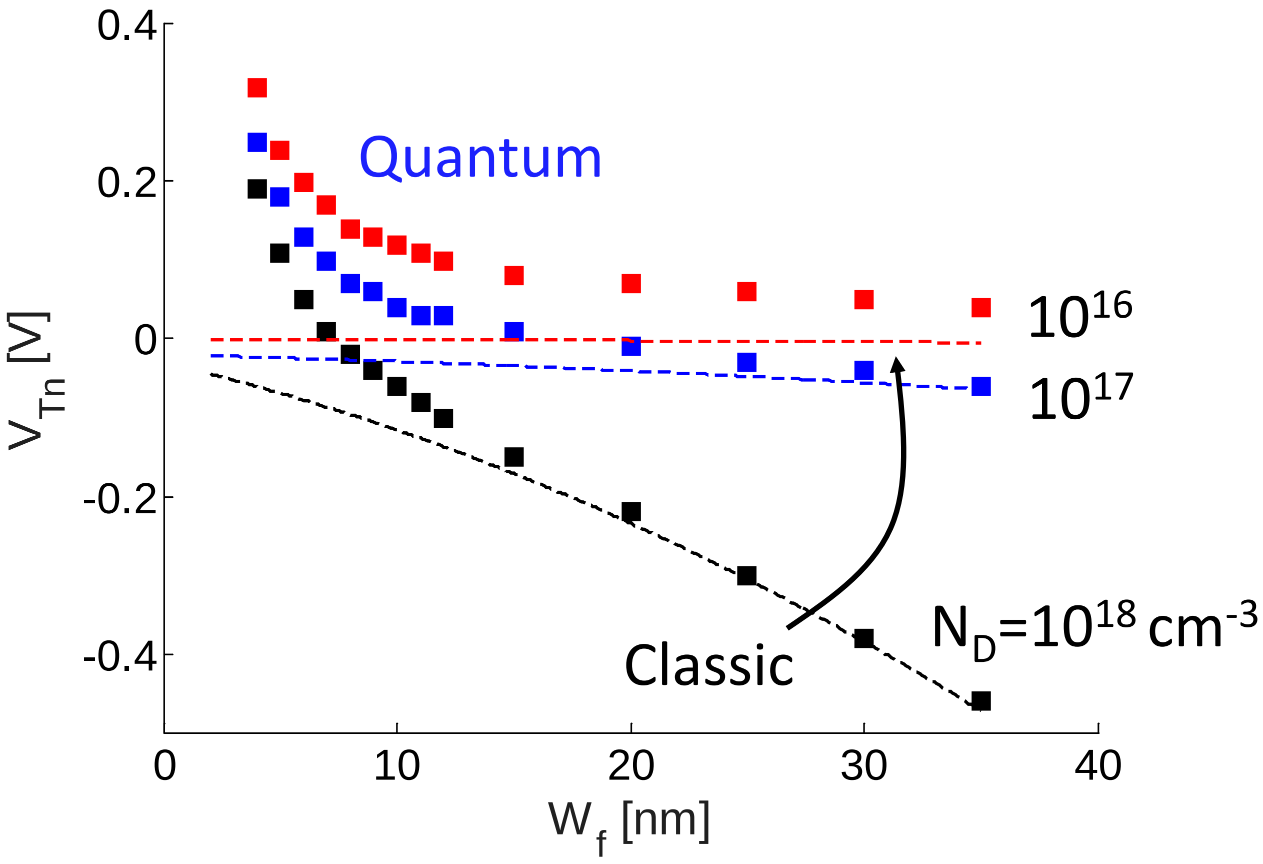


$\overline{W}_f = W_f + 4$ nm



V_T vs. $\overline{W}_f$ match for both sidewall slopes

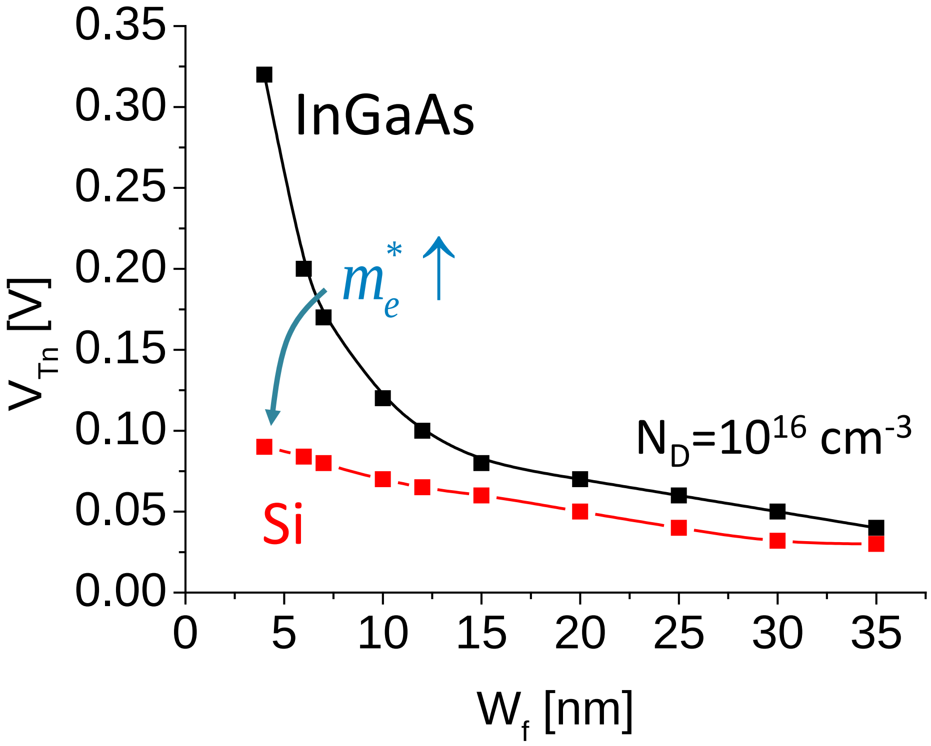
Impact of W_f on V_T: effect of doping



- Reduced doping (inv. mode) → reduced V_T variation
- Strong quantum ΔV_T for W_f<10 nm regime

Impact of W_f on V_T: comparison with Si

Self-consistent P-S simulations:



V_T of InGaAs finFETs with W_f<10 nm:

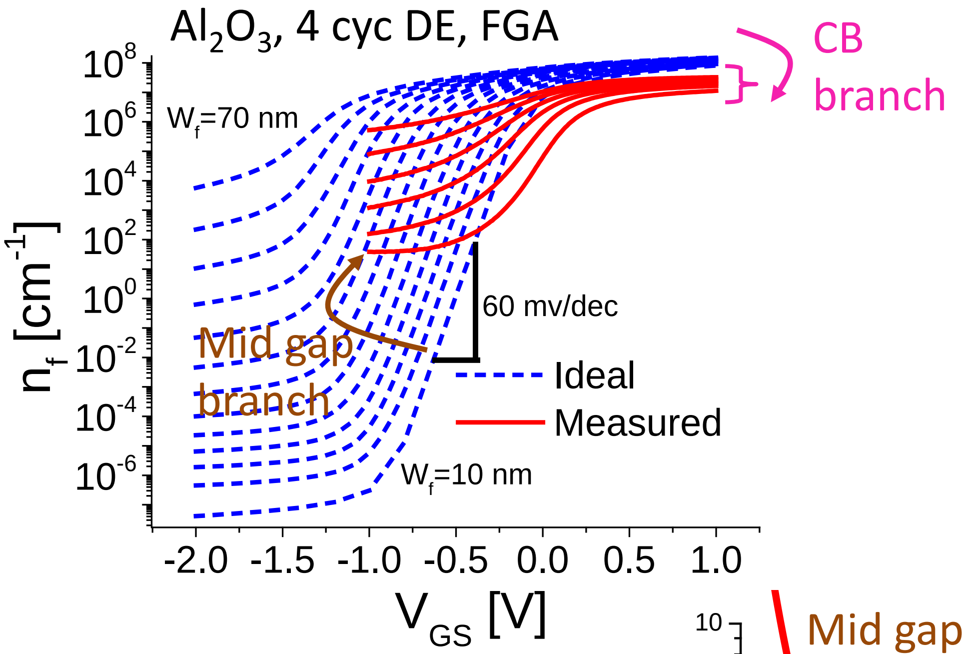
- ~4x more sensitive to W_f than Si!
- due to quantum effects

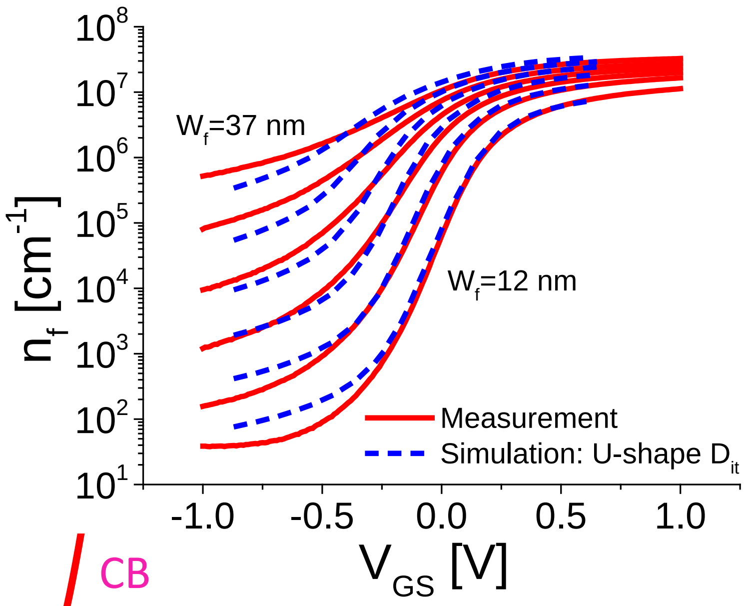
Conclusions

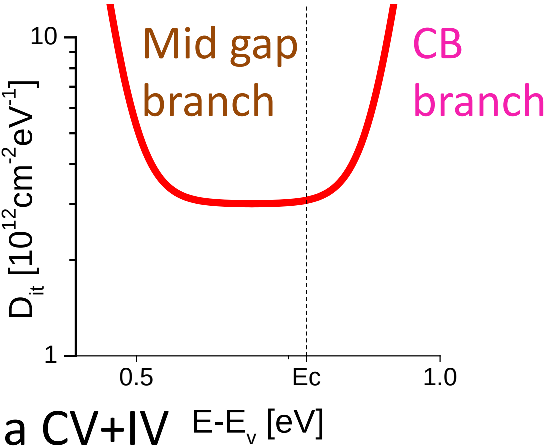
- InGaAs finFETs with W_f<10 nm demonstrated experimentally
- Observation of quantum size effects in sub-10 nm fins
- Implication for manufacturing control in future nm-scale InGaAs finFETs

Thank you !

Sidewall D_{it} profile



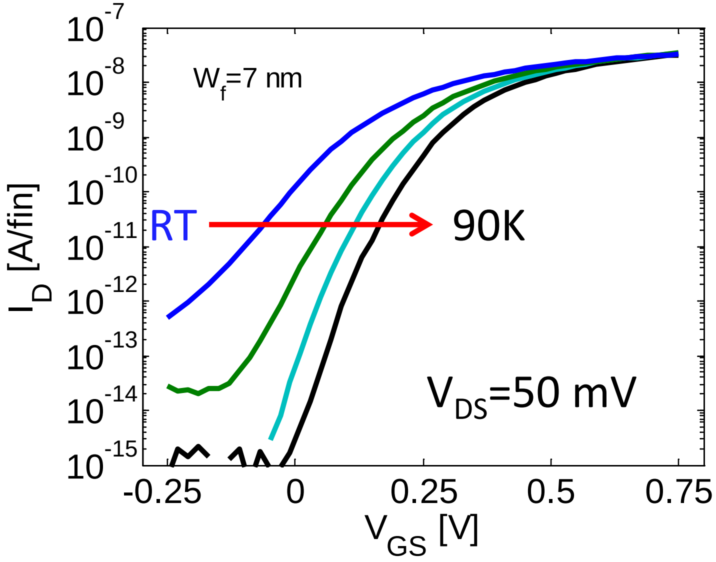




Vardi, DRC 2014

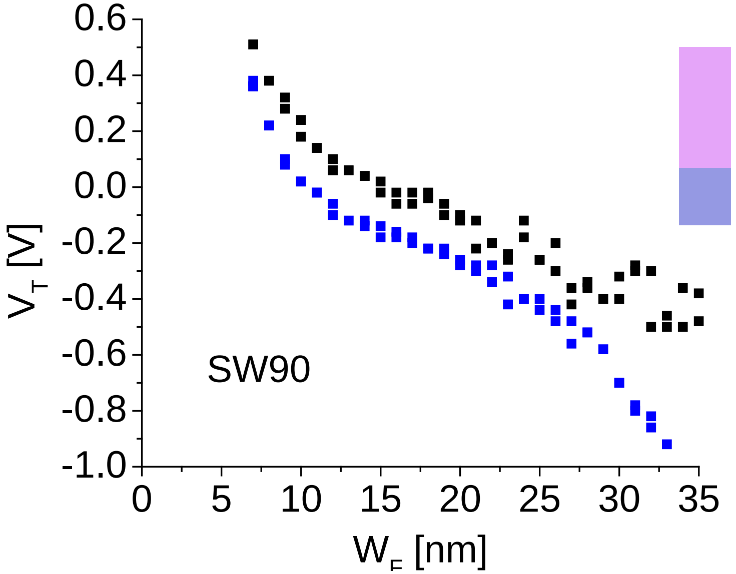
- Fitting with μ_{max} extracted via CV+IV
- U-shape D_{it} profile provides excellent agreement with measurements for the entire W_f range.
- At the flat minima – D_{it} level of $3x10^{12}$ $cm^{-2}eV^{-1}$

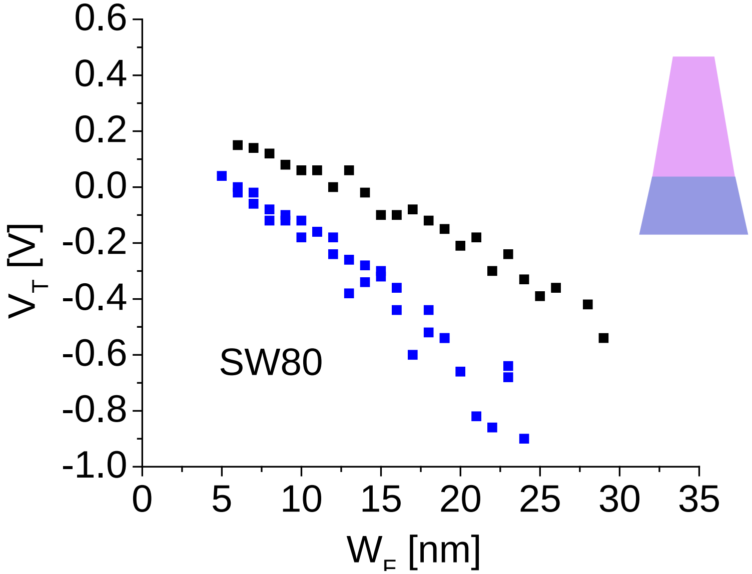
Low-temperature measurements



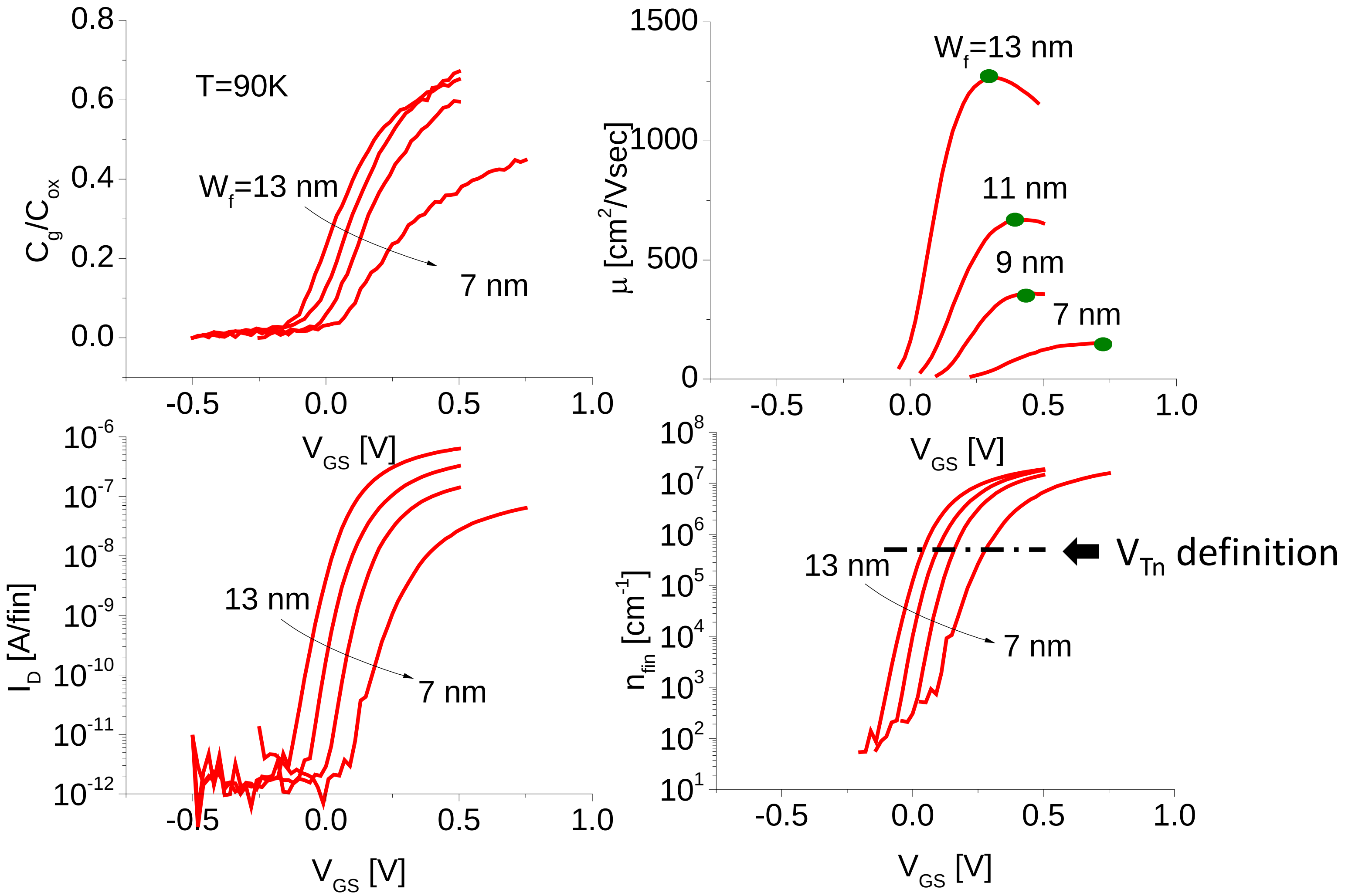
as T↓ →

- D_{it} impact ↓
- Rigid $\Delta V_T > 0$
- Strong sensitivity of V_T to W_F for SW90 maintained



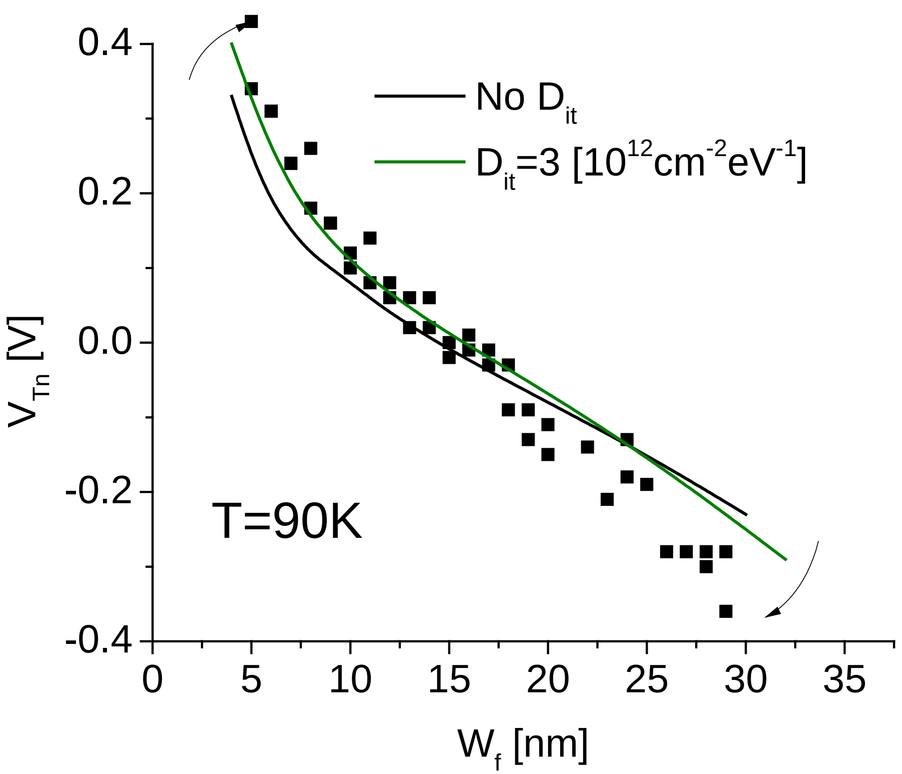


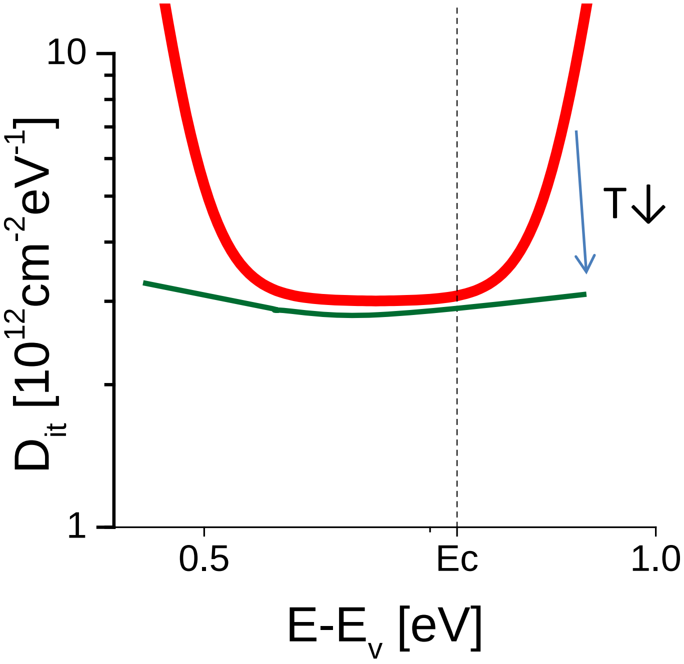
Subthreshold carrier concentration at 90K



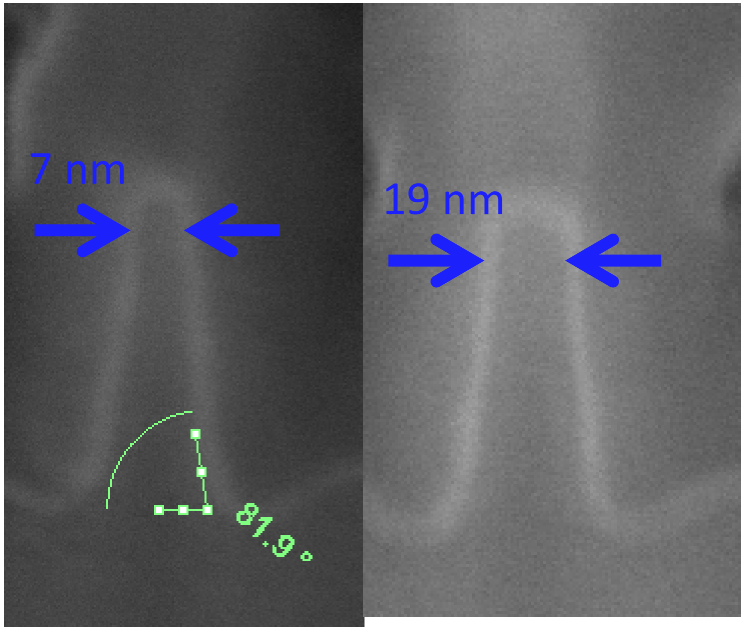
- CV+IV → μ(V_{GS})
- Use $μ_{max}$ to transfer subthreshold characteristics to n_{fin}

Effect of D_{it} on V_T-W_F dependence

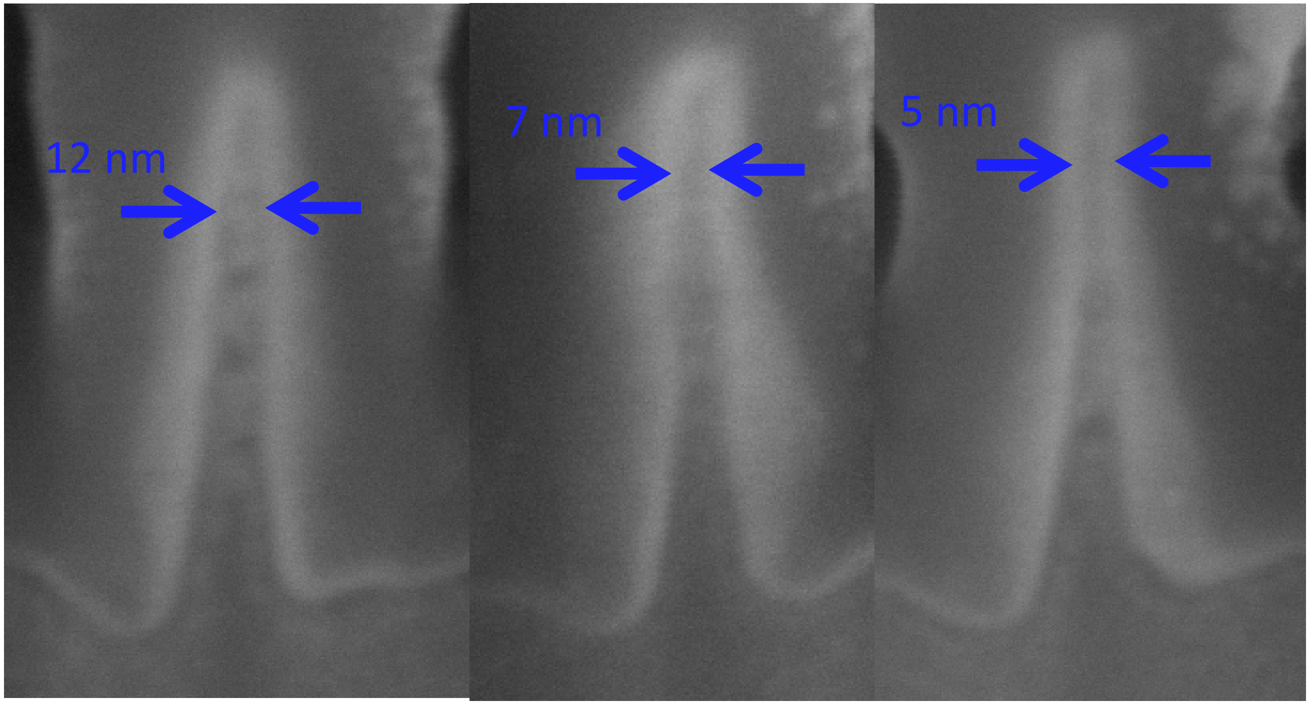




SW80 - different W_F



SW90 - different W_F



Sub T carrier concentration

$$I_D = \frac{W}{L} D_e \frac{kT}{q} C_T \exp\left[\frac{q\left(V_{GS} - V_T\right)}{nkT}\right]\left(1 - \exp\left[-\frac{qV_{DS}}{nkT}\right]\right)$$

$$I_D = \frac{W}{L} \mu_e \left(\frac{kT}{q}\right)^2 C_T \exp\left[\frac{q\left(V_{GS} - V_T\right)}{nkT}\right]\left(1 - \exp\left[-\frac{qV_{DS}}{nkT}\right]\right)$$

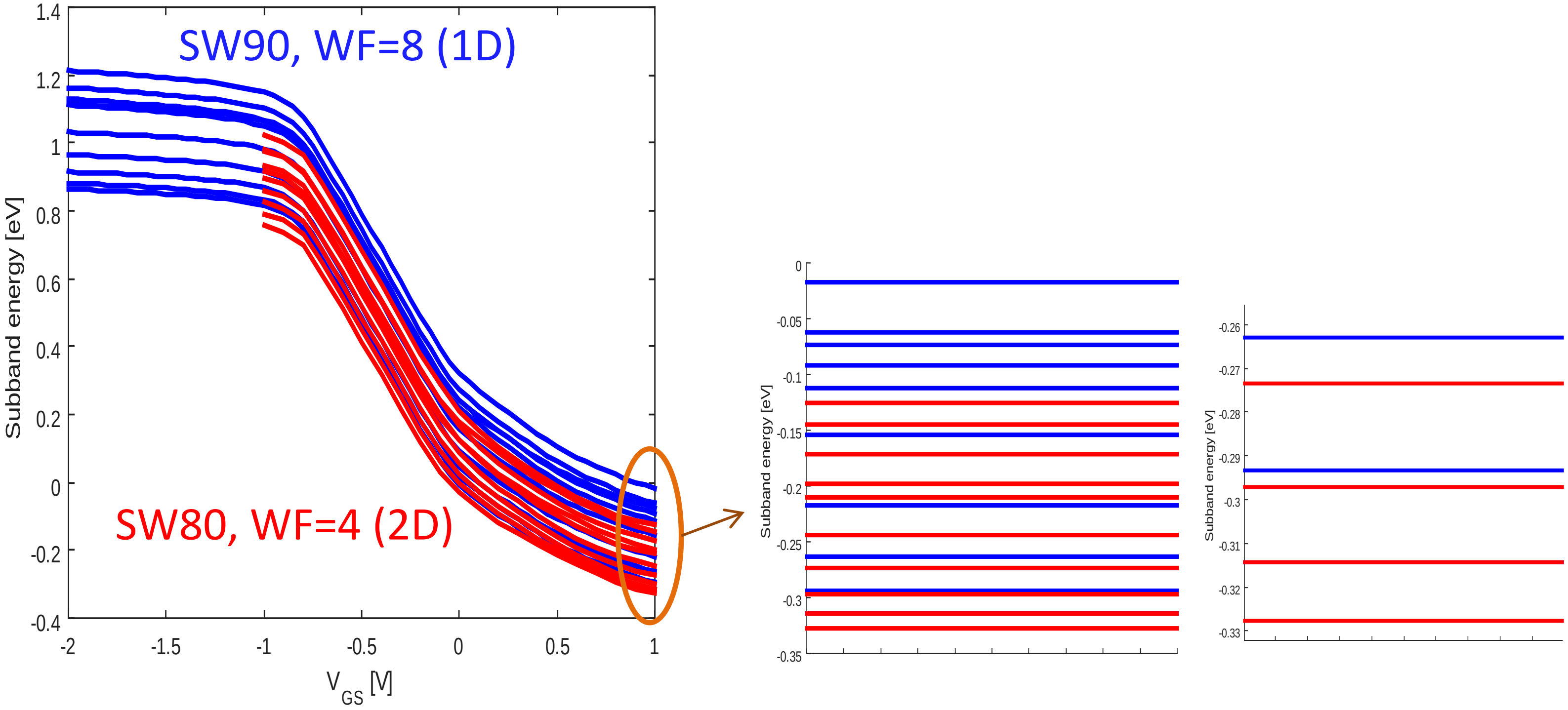
$$I_D = \frac{W}{L} \mu_e \left(\frac{kT}{q}\right) Q\left(V_{GS}, V_{DS}\right)$$

$$\rightarrow Q\left(V_{GS}, V_{DS}\right) = \frac{I_D L}{W \mu_e}\left(\frac{q}{kT}\right)$$

For long channel at small V_{DS}, the channel charge (source side) is:

$$Q\left(V_{GS}\right) = \frac{I_D L}{W \mu_e}\left(\frac{q}{kT}\right)$$

Sub-bands spectrum



SW80 eigs are lower with smaller dispassion (larger density of states)